

First Generation
Single CPU - multiple line cards
Single electrical backplane

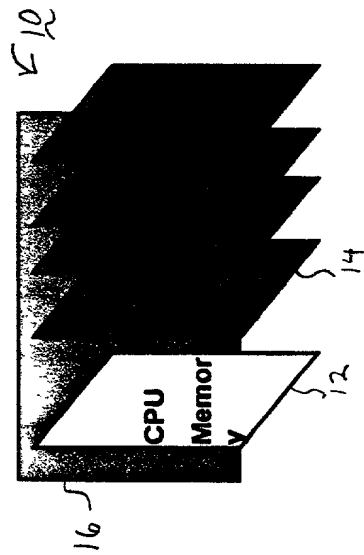


Fig 1A

Second Generation
One CPU per Line Card
Central Controller for Routing Protocols

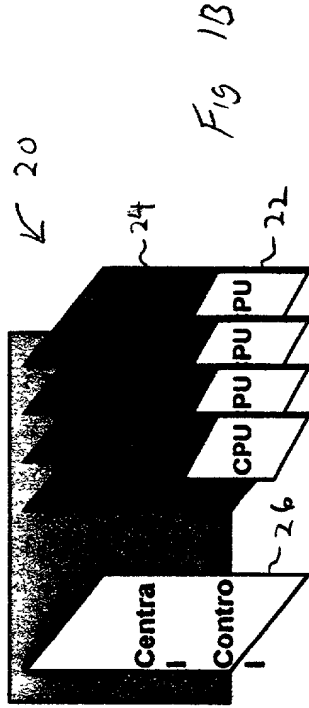


Fig 1B

Fourth Generation
Multiple shelves of Line Cards
Centralized Switch Fabric

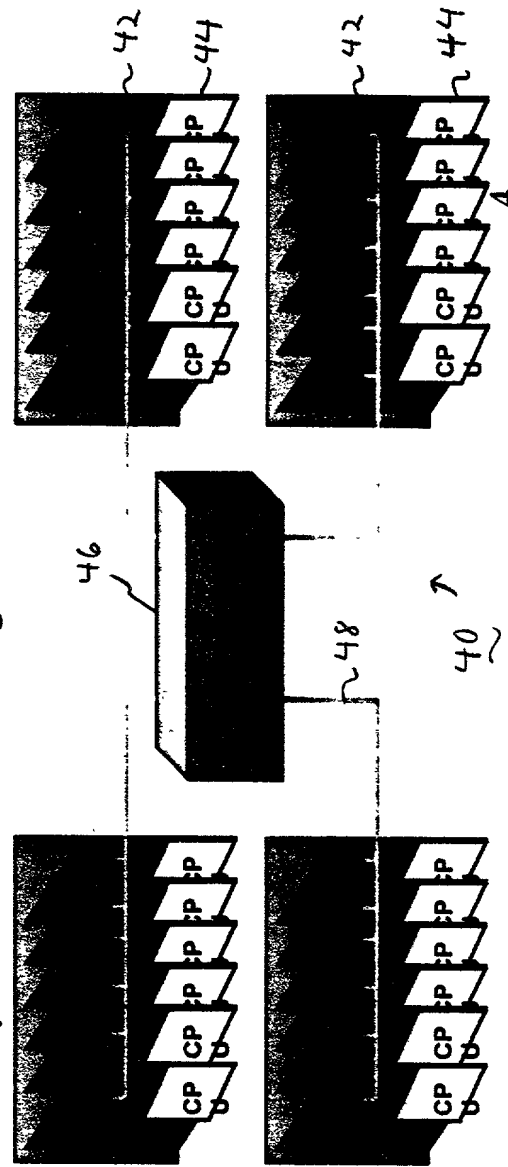


Fig 1D

Third Generation
One CPU per Line Card
Central Controller for Routing Protocols
Switch Fabric for inter-connection

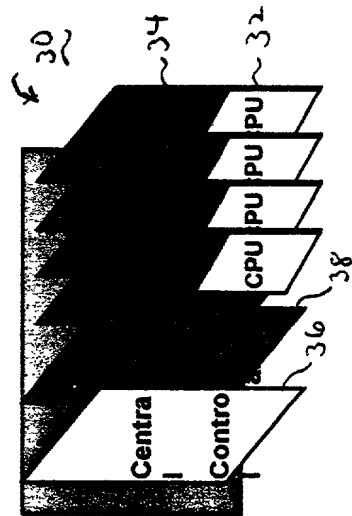


Fig 1C

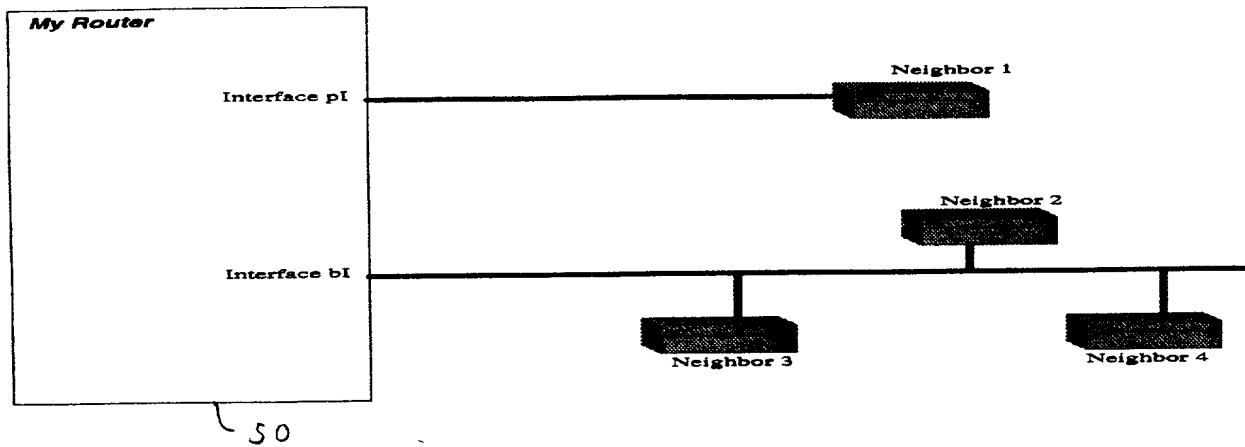


FIG. 2

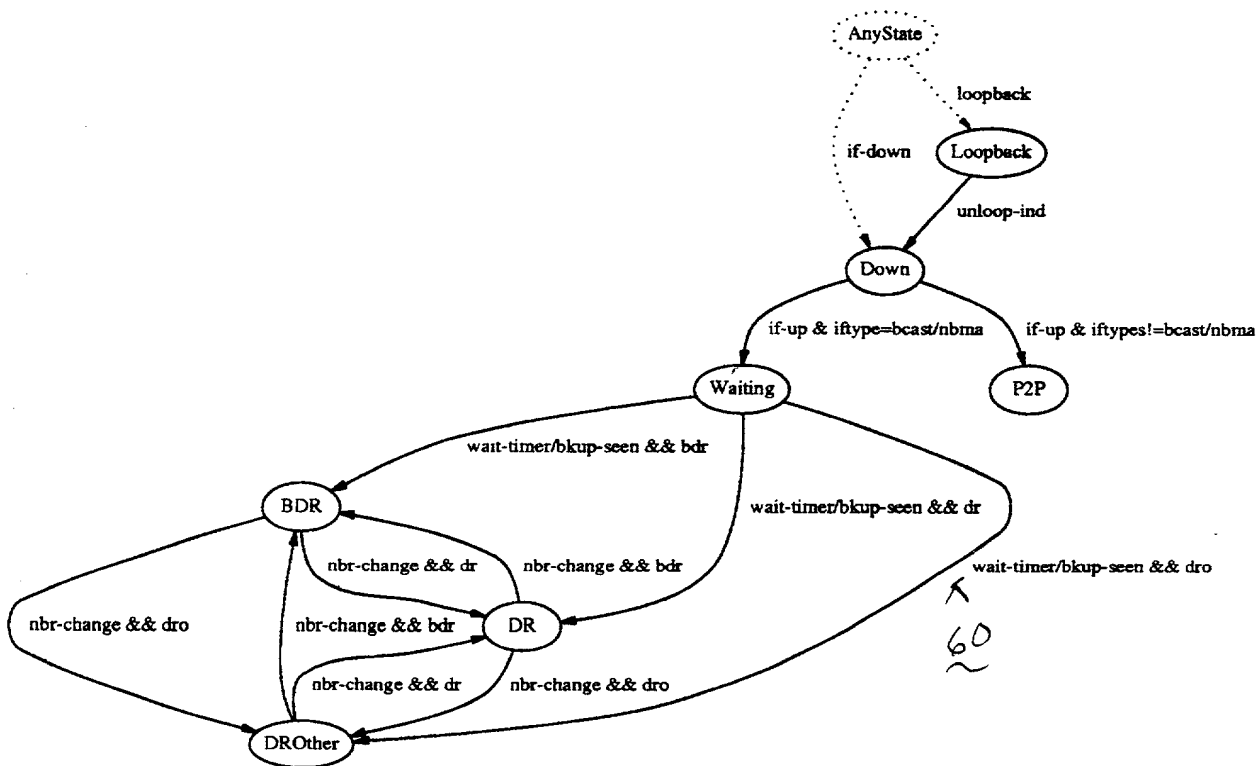


Fig. 3 OSPF Interface FSM

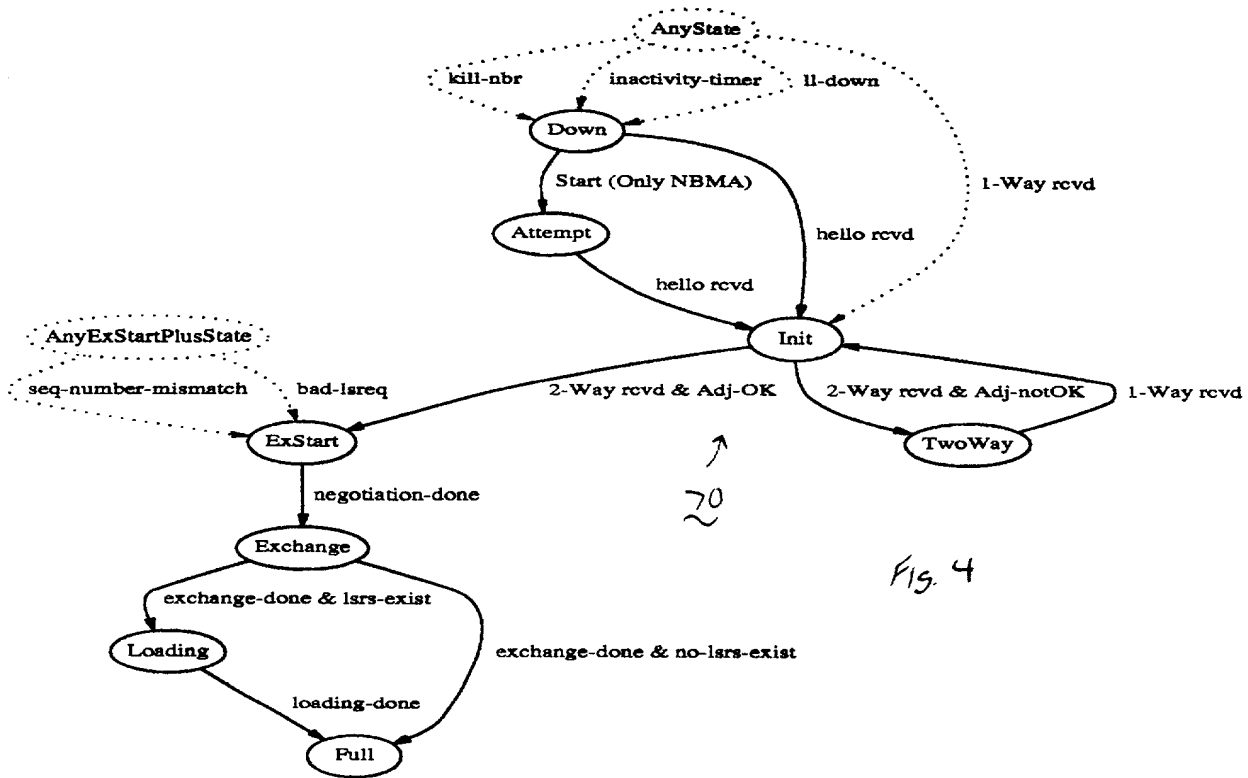
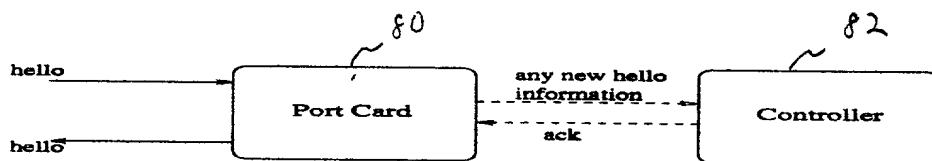


Fig. 4



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Fig. 4. Distributed Hello Processing

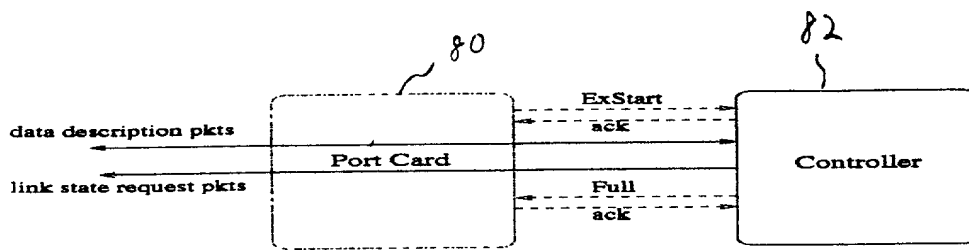


Fig. 6. Initial DB Exchange

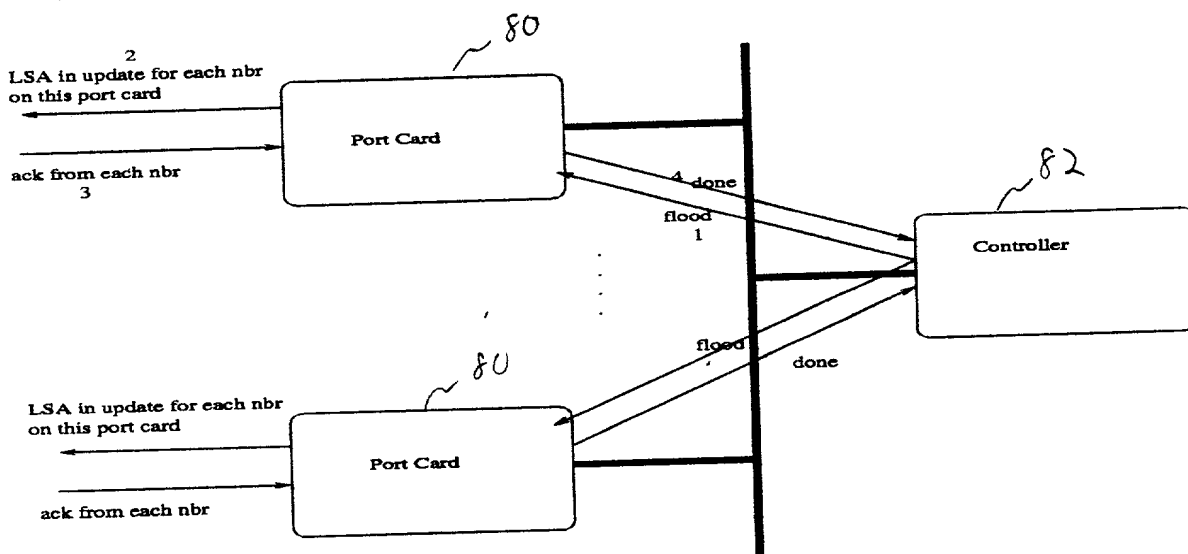


Fig. 7

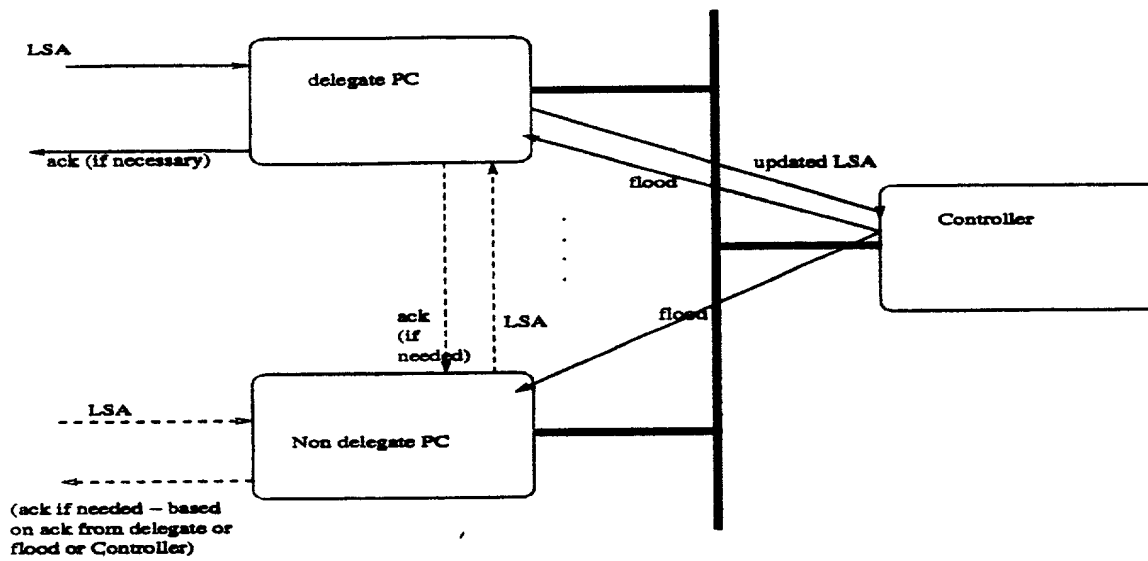


Fig. 8. Distributed Processing of Incoming LSA Updates